REMARKS

Claim 11 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Go (USPN 6,320,566). Applicant traverses this rejection because the cited prior art reference does not disclose a timing controller that outputs data signals of even-numbered dots and data signals of odd-numbered dots, while displacing the phase of the data signals of even-numbered dots and odd-numbered dots by 180 degrees.

The examiner asserts that the timing controller disclosed by Go corresponds to the timing controller recited in claim 11. The timing controller of Go, shown as controller IC (integrated circuit) 100 in Fig. 10, outputs two clock signals FD1 and FD2, where the phase of the clock signal FD1 is displaced 180 degrees with respect to clock signal FD2. However, the controller IC does not output video signals for even-numbered dots and odd-numbered dots, displaced from one another by 180 degrees.

Instead, as shown in Fig. 10, a data driver IC 120 receives signals S1 and S2 from the controller IC 100, where signal S1 is a data signal for odd-numbered dots, and signal S2 is a data signal for even-numbered dots. As shown in Fig. 11, signals S1 and S2 are in phase with one another. Next, signal S1 and clock signal FD1 are used as inputs to a first XOR logic gate 160, producing output signal S'1. Similarly, signal S2 and clock signal FD2 are used as inputs to a second XOR logic gate 160, producing output signal S'2. Signals S'1 and S'2 are 180 degrees out of phase with one another. Accordingly, Go discloses that the data driver IC 120, produces video signals that are 180 degrees out of phase with respect to one another, and not the controller IC 100. Because the Go reference fails to disclose a

controller IC that outputs data signals for odd-numbered dots and data signals for even-numbered dots, while displacing the phase between the data signals by 180 degrees, as required by claim 11, applicant requests withdrawal of the rejection.

Claims 1 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Go in view of Misawa et al. (USPN 5,616,936). Applicant traverses the rejection because Go and Misawa, taken alone or in combination, fail to disclose or suggest a load means for making a load capacitance of a second clock signal line equal to or substantially equal to a load capacitance of a first clock signal line.

The examiner asserts that Go shows, in Figs. 10 and 12, that a second clock signal line is arranged to be parallel with a first clock signal line. The examiner then acknowledges that Go does not disclose a load means for making the load capacitance of the second clock line equal to or substantially equal to the load capacitance of the first clock line. Instead the examiner cites Misawa for disclosing this feature.

Misawa is directed to an active matrix assembly with signal line crossing to equalize stray capacitance. Misawa discloses that a first clock signal line crosses a second clock signal line so that a capacitance between the first clock signal line and a signal bus is substantially equal to a capacitance between the second clock signal line and the signal bus. Fig. 11A of Misawa shows that a first clock line 218 and a second clock line 219 are "twisted, crossing near their centers" (see Misawa, col. 12, lns. 31-32). This configuration ensures that the stray capacitance formed between each clock line 218, 219 and a video signal bus 217 are equal. That is, the stray capacitances formed between each of the clock

lines and the video signal bus are only equal when the clock lines are not parallel to one another. Moreover, the examiner asserts that it is presumed that the clock lines of Misawa are arranged in a twisted helical manner. While this may be the case, two lines arranged in a twisted helical nature are not arranged in parallel, as required by claim 1. Thus, Misawa teaches that equivalent stray capacitance is maintained by ensuring that the clock lines 218, 219 are not parallel. Accordingly, there is no motivation to combine the references as suggested by the examiner. For this reason, applicant respectfully requests withdrawal of the rejection of claim 1 and its associated dependent claims.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Go in view of Jeon et al. (USPN 6,320,566). Applicant traverses this rejection because the cited references do not disclose or suggest data driver ICs receiving first and second clock signals and a selection signal as inputs, so that each data driver IC can selectively latch data signals with either the first or second clock signal.

The examiner acknowledges that Go does not disclose this feature, and cites Jeon as disclosing it. Jeon discloses a shift register 164 that includes eight stages SRH1 to SRH8 corresponding to eight data line blocks, and a ninth stage SRH9 that operates as a control stage. The shift register 164 receives as inputs a first clock signal, a second clock signal, and a block selection start signal. Odd stages of the shift register SRH1, SRH3, SRH5, SRH7 provide an output matching the first clock signal, while even stages of the shift register SRH 2, SRH4, SRH6, SRH8 provide an output matching the second clock signal. The outputs from each stage of the shift register SRH1 to SRH8 are provided to block selection

terminals of respective data line blocks, and serve as the enable signals for each line block. Accordingly, each line block is provided only with the enable signal, and not with the first and second clock signals. Moreover, because the enable signal provided to each block corresponds to a single clock signal, the data line block can only latch data with the corresponding clock signal (i.e., odd-numbered data blocks can only latch data with the first clock signal, and even-numbered data blocks can only latch data with the second clock signal).

In contrast, claim 7 recites that each data driver IC receives first and second clock signals and a selection signal as input. The data driver IC selects the first or second clock signal based on the selection signal, and can selectively latch data signals with the first or second clock signal. Fig 17 of the present invention shows a display panel using data driver ICs 96, and Fig. 18 shows a block diagram of an example construction of each of the data driver ICs. As shown in Figs. 17 and 18, each of the data driver ICs independently receives clock signals CLK and /CLK, and selection signal SL as inputs. Logic gates 97-101 are used to select one of the input clock signals to be used as an internal clock signal I-CLK. Each of the data driver ICs 96 also includes a data latch 102 alternately latching data for odd-numbered dots or even-numbered dots in synchronism with the internal clock signal. Because Go and Jeon fail to disclose or suggest a data driver IC as recited in claim 7, applicant respectfully requests withdrawal of the rejection of claim 7.

Claims 9 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Go in view of Jeong (USPN 6,335,721). Regarding claim 9, applicant traverses the

rejection because the cited prior art references, taken alone or in combination, fail to disclose or suggest a sampling memory that outputs saved data signals to a digital to analog converter, as is now recited in claim 9.

Go shows, in Fig. 12, a data driver IC includes a first data latch 200. However, as acknowledged by the examiner, Go fails to disclose a second data latch or a sampling memory. Instead, the examiner relies on Jeong to disclose these features.

Jeong is directed to an LCD source driver, and shows a data driver IC in Fig. 4 and 5. Jeong also shows, in Fig. 2, sample & hold circuits 56 and 70, which receive, as inputs, analog video signals that have been converted from digital signals by digital to analog converters 54 and 68, respectively. The sample & hold circuits 56 and 70 then output the analog signals to an output buffer circuit 64, which functions as a type of multiplexer (see Jeong, col. 2, lns. 3-11). That is, Jeong merely discloses a sample & hold circuit that outputs analog signals to a multiplexer, and not a sampling memory that that outputs data signals to a digital to analog converter, as recited in claim 9.

In contrast, claim 9 of the present application recites a sampling memory that outputs stored data signals to a digital to analog converter. As shown in Fig. 12 of the present application, a sampling memory 92 receives and stores data signals for both even-number dots and odd-number dots as digital data, and then outputs the stored signals to a digital to analog converter 94. That is, the sampling memory recited in claim 9 receives, as inputs, the outputs of first and second latches, and provides an output to a digital to analog

converter. Since Go and Jeong, taken alone or in combination, do not disclose or suggest this feature, applicant respectfully requests withdrawal of the rejection of claim 9.

Regarding claim 10, applicant traverses the rejection because Go and Jeong fail to disclose or suggest a selection signal that is used as the basis for selecting a first or second clock signal.

The examiner cites Go as disclosing a data driver IC, but acknowledges that the data driver IC of Go does not include a selection signal that is used to select a first or second clock signal, allowing the data driver IC to selectively latch data signals with either the first or second clock signal. Instead, the examiner relies on Jeong to teach this feature.

Jeong discloses a multiplexer used in the control logic of an LCD source driver. The multiplexer receives as inputs even channel video and odd channel video, and a polarity control signal. The polarity control signal is used as a selection, determining whether the multiplexer outputs the even channel video signals or the odd channel video signals. Thus, the polarity control signal disclosed by Jeong merely selects between even or odd channel data, and not between first and second clock signals, as recited in claim 10. Moreover, Jeong shows, in Fig. 5, a plurality of latches 101-104 for latching video data. The latches 101 and 103 are connected to the first clock signal CLK1, while the latches 102 and 104 are connected to the second clock signal CLK2. Thus, it is clear that Jeong does not disclose selectively latching data according to CLK1 or CLK2, but rather latching data with both signals. Because Jeong fails to disclose or suggest a selection signal used as the basis for selecting a first or second clock signal and selectively latching data with the first or second

clock signal, as recited in claim 10, applicant requests withdrawal of the rejection of claim 10.

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Go in view of Ogata et al. (JP 407329337). Applicant traverses the rejection because Go and Ogata fail to disclose or suggest that output pins for a timing controller are arranged so that data signal of an odd-number dot of each bit of each color and a data signal of an even-numbered dot of the same bit are adjacent to one another.

The examiner acknowledges that Go does not disclose this feature, and instead relies on Ogata. Ogata merely discloses that a data signal DATA1 having odd bits (1, 3 ... n-1) is output through a component 21, while a data signal having even bits (2, 4 ... n) is output through an adjacent component 22. However, it is clear from Fig. 1 of Ogata that for an output pin of each bit of the data signal having odd bits, a corresponding output pin of a bit of the data signal having even bits is not adjacent thereto.

In contrast, the present specification discloses that a dot is made up of 3 colors, and that each of those colors is specified using 8 bits numbered 0 through 7. Bits are identified according to color, bit number, and whether a dot is even or odd. For example, the first bit of the red color portion of an odd dot is referred to as R0O, while the first bit of the red color portion of an even dot is referred to as R0E. Fig 15 of the present application shows an arrangement of the output pins of a timing controller 108. It is clear from the figure that for each output pin of an odd dot, a corresponding output pin of an even dot is adjacent thereto. For example, the output pin for bit R7E is adjacent to the output pin for bit

R7O, the output pin for bit G0E is adjacent to the output pin for bit G0O, and so on. Because Go and Ogata, taken alone or in combination, do not disclose this configuration, applicant requests withdrawal of the rejection of claim 12.

Claims 2-4 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Go and Misawa in view of either Toyoshima et al. (USPN 6,795,049), Drake et al. (USPN 6,339,413), or Ogata. Claims 2-4 and 6 ultimately depend from claim 1, and thus include all the features of claim 1, plus additional features. Applicant traverses the rejection of these claims for the reasons recited above regarding claim 1, and because Toyoshima, Drake and Ogata do not remedy the deficiencies of Go and Misawa identified above with respect to the rejection of claim 1. Accordingly, withdrawal of the rejections of claims 2-4 and 6 is respectfully requested.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Go, in view of Jeon and Ogata. Claim 8 depends from claim 7, and as such, includes all features of claim 7, plus additional features. Thus applicant traverses the rejection for the reasons cited above with respect to claim 7, and because Ogata does not remedy the deficiencies identified above regarding the rejection of claim 7.

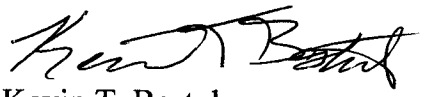
For all of the foregoing reasons, applicant submits that this application is in condition for allowance, which is respectfully requested. The examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

If a Petition under 37 C.F.R. §1.136(a) for an extension of time for response is required to make the attached response timely, it is hereby petitioned under 37 C.F.R.

§1.136(a) for an extension of time for response in the above-identified application for the period required to make the attached response timely. The Commissioner is hereby authorized to charge fees which may be required to this application under 37 C.F.R. §§1.16-1.17, or credit any overpayment, to Deposit Account No. 07-2069.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 

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